



**SIDDARTHA INSTITUTE OF SCIENCE AND TECHNOLOGY :: PUTTUR
(AUTONOMOUS)**

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QUESTION BANK

Subject with Code : Advanced Digital system design(18EC4001)

Course & Branch: M.Tech – (DECS)

Year & Sem: I-M.Tech & I-Sem

UNIT-I

DESIGN OF DIGITAL SYSTEMS & SEQUENTIAL CIRCUIT DESIGN

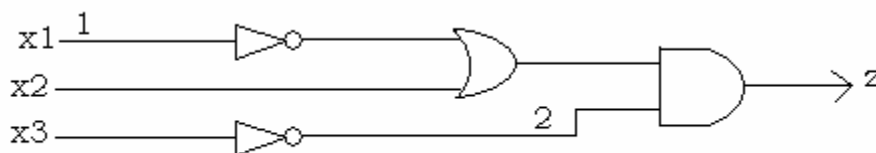
1. a). Draw an ASM chart of JK flip-flop. [5M]
b). Write an example about state reduction of state tables. [5M]
2. Design a logic circuit which generates the square of a given three bit binary number. Realize the design using ROM. [5M]
3. a). Draw an ASM chart to design a sequence detector which can detect 01101 sequences. For all other bit patterns there is no change in output. [5M]
b). Explain the use of HDL in digital system design. [5M]
4. a). Design a logic circuit which generates the square of a given three bit binary number. Realize the design using ROM. [5M]
b). Describe the rules for state assignment. Give an example? [5M]
5. a). With an example, explain the use of ASM charts in the design of digital circuits. [5M]
b). Discuss in detail about the following.
i). Reduction of state tables ii). State assignment procedure [5M]
6. a). Develop an ASM chart of D flip flop and realize it using only NAND gates. [5M]
b). Discuss about reduction of state tables and state assignments. [5M]
7. a). Draw the general structure of an FPGA and explain how a logic- function can be realized on FPGA with a simple example. [5M]
b). Write HDL Program for J-K-flip flop in structural model. [5M]
8. a). Describe some important features of an FPGA and a CPLD. [5M]
b). With an example, explain how an FPGA is useful in the design of a digital circuit. [5M]
9. a). Draw the general structure of a CPLD and explain how a logic function can be realized on CPLD with simple example. [5M]
b). Write HDL Program for D-flip flop in behavioral model. [5M]
10. Design a digital system by using following [10M]
a). Chart implication method b). Row matching method.

Prepared by: **M.Vijaya Lakshmi.**

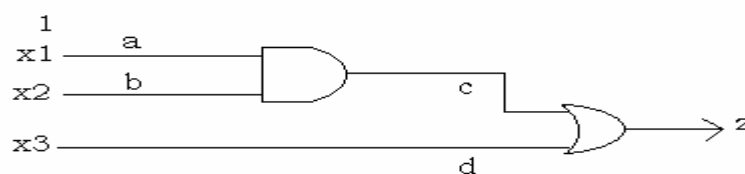
UNIT-II

FAULT MODELING & TEST GENERATION

1. a). Explain the Stuck at faults with an example. [5M]
 b). Draw the circuit which realizes the logic function $z = x_1 x_2 + x_3 x_4$ using AND and OR gates. For the circuits realized above, determine a test vector which denotes SA0 fault on the line 'x2'. [5M]
2. a). Discuss about any one method of fault diagnosis in sequential circuits using an example. [5M]
 b) Define a diagnosable sequential machine and how it can be constructed. [5M]
3. a). Explain the Boolean difference method with an example. [5M]
 b). Explain bridge fault model. [5M]
4. a). Clearly, distinguish between Meelay and Moore machines with examples. [5M]
 b). Find the test vectors of all SA0 and SA1 faults of the circuit function. [5M]
 $F = x_1 x_2 + x_1 x_3' x_4' + x_2 x_4$ using Kohavi algorithm. [5M]
5. Explain the procedure of designing a fault detection experiment with the help of an example. [10M]
6. a). Explain the following types of faults. [5M]
 - i). Stuck at faults
 - ii). Bridge faults
 b). With an example, Explain the procedure involved in the path sensitization technique. [5M]
7. What is the significance of Kohavi algorithm? Explain how it is useful in the detection of faults in digital circuits. [10M]
8. a). Draw the circuit which realizes the function $f(x) = (x_2 + x_3) + x_1' x_4$ using AND-OR gates using Boolean difference method obtain the test set to detect Sao fault on input line x1 of the circuit. [5M]
 b). Using the path-sensitization method and Boolean difference method find the test vectors for SA0 fault on input line 1 and SA1 fault on the internal line 2 of the circuit shown in figure. [5M]



9. a). Draw the table giving the set of all possible single stuck faults and the faulty and fault-free responses and also construct the fault cover table for the circuit in figure. [5M]



- b).Discuss the different types of faults in a digital circuits. [5M]
- 10.a). Discuss about any one method of fault diagnosis in sequential circuits using an example. [5M]
- b). Define a diagnosable sequential machine and how it can be constructed. [5M]

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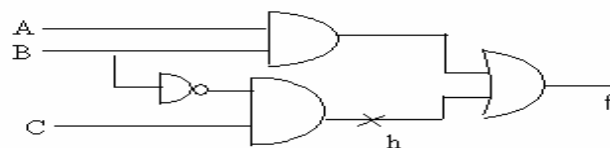
UNIT-III

TEST PATTERN GENERATION

1. a). Explain transition counting testing with an example. [5M]
 b). Discuss in brief about D- algorithm.
2. Construct a fault detection experiment for the machine if the that is entirely present, that is with no initial adaption part. [10M]

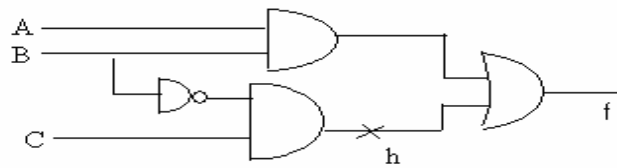
PS	NS,Z	
	X=0	X=1
A	D,0	C,0
B	C,0	D,0
C	A,0	B,0
D	D,1	A,0

3. a). Explain briefly podem with an example [5M]
 b). Give the classification of faults that may occur in digital circuits with examples, [5M]
4. Explain signature analysis with example. [10M]
5. a). Explain the procedure involved in D- Algorithm with an example. [5M]
 b). Find the minimized PLA of the following output Boolean function by a PLA minimizer.
 $f1 = (2,4,5,6,7,10,14,15)$: $f2 = (4,5,7,11,15)$ [5M]
6. a). What are the difference between PLA and PAL. [5M]
 b). Explain how faults are detected in PLA. [5M]
7. a) Apply D-algorithm to detect h SA0 fault in the given circuit and derive the test vectors. [5M]



- b) How a transition count is used to test faults. [5M]
8. a) Describe the algorithmic steps involved in PODEM. [5M]
 b) With an example, explain the transition count testing method. [5M]
9. With an example, explain the test vector for bridging faults. [10M]

10. a) Apply D-algorithm to detect the SA1 fault in the given circuit and derive the test vectors. [5M]



b). Explain in detail different test pattern generation method. [5M]

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UNIT -IV**PROGRAMMING LOGIC ARRAYS & FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS**

1. a). Realize F1 and F2 using PLA. Give the PLA table and interconnection diagram for the PLA. [5M]
 $F1(a,b,c,d) = \sum m(1,2,4,5,6,8,10,12,14)$ $F2(a,b,c,d) = m(1,2,4,5,6,11,12,14,15)$
 b). List the advantages of PLA. [5M]
2. a). Explain about PLA folding. [5M]
 b). Plot following PLA on the map. Identify the undetectable faults. Determine minimal test for all detectable test for all detectable faults. [5M]

X1	X2	X3	X4	Z1	Z2
0	2	2	1	1	0
2	1	1	2	1	1
0	1	2	1	0	1

3. Give the PLA realization of the following functions using a PLA with 5 inputs, 4 outputs and 8 AND gates.
 $F1(a,b,c,d) = \sum m(0,1,2,3,11,12,13,14,15,16,17,18,19,27,28,29,30,31)$
 $F2(a,b,c,d) = \sum m(4,5,6,7,8,9,10,11,20,21,22,23,30)$ [10M]
4. a). Design a 3 bit BCD to grey code converter and realize the circuit using PLA and then show that how folding will reduce the number of cross points given on the PLA. [5M]
 b). Describe the advantages of PLA minimization and folding. [5M]
5. a) List out and explain briefly about the faults that may occur in PLAs. [5M]
 b). Briefly describe about PLA folding. [5M]
6. a). With examples, explain in detail about various types of cross point fault that occur in PLAs. [5M]
 b) With an example, explain how test generation can be achieved in testing a PLA. [5M]
7. a). Explain the different types of fault models and fault types in a PLA. [5M]
 b). Discuss briefly, the steps involved in the PLA folding algorithm 'COMPACT'. [5M]
8. Discuss about state Identification experiment and fault detection experiment. [10M]
9. Find the shortest homing sequence for the machine shown in table. Let $n=4$. [10M]

PS	NS,Z		
	I1	I2	I3
S1	S1,0	S1,0	S1,0
S2	S3,0	S2,0	S2,0
S3	S2,0	S4,0	S3,0
S4	S4,0	S3,0	S4,0

10. a). Explain the different types of fault diagnosis methods in sequential circuits. [5M]
- b). Explain the procedure of designing a fault detection experiment with the help of an example. [5M]

Prepared by: **M.Vijaya Lakshmi.**

UNIT -V

PLA TESTING & ASYNCHRONOUS SEQUENTIAL MACHINE

1. a).With an example, explain how test generation can be achieved in PLA testing. [5M]
 b).Explain how faults are detected in PLA. [5M]
2. a).Explain following with example. [5M]
 i). Flow tables
 ii). State Reduction
 b).Write a brief note on minimal closed covers? [5M]
3. a).With respect to an asynchronous sequential machine, explain about minimal closed corners. [5M]
 b). Define the races and cycles in sequential circuits? [5M]
4. Write short notes on the following.
 a) Capabilities and limitations of FSM [4M]
 b) Transition checks approach in sequential circuits. [3M]
 c). Minimum closed covers [3M]
5. Explain following with an example.
 i). Fundamental mode model [5M]
 ii). Hazards [5M]
6. a).Explain briefly, the occurrence of various types of hazards in digital circuits. [5M]
 b).Implement a hazard free circuit for the following function: [5M]

$$f(ABCD) = A'BC' + A'B'C + CD' + AC$$
7. Write a short note on.
 i). Design for testability [5M]
 ii). Field programmable gate arrays [5M]
8. Give a state assignment without critical races to each of the following asynchronous machine shown in figure. [10M]

q \ x	I ₀	I ₁	I ₂	I ₃
A	(A)	C	(A)	B
B	A	(B)	A	(B)
C	(C)	(C)	E	D
D	C	B	(D)	(D)
E	(E)	F	(E)	D
F	E	(F)	A	B

9. Construct the fault detection experiment for the machine shown below.

[10M]

PS	NS,Z	
	X=0	X=1
A	B,0	C,1
B	C,0	D,0
C	D,1	C,1
D	A,1	B,0

10. Write short notes on the following.

- Capabilities and limitations of FSM
- Transition check approach in sequential circuits

[5M]

[5M]

Prepared by: **J.Rajanikanth**